RTC6705 CMOS 5.8GHz Band FM Transmitter

Product Description

The RTC6705 is a wide-band FM transmitter intended for the application on 5.8GHz bands FM transmission. This chip includes a 5.8GHz band RF modulator, two channels of audio modulator and internal power amplifier with +13dBm power output referred to external matching network. The 5.8GHz band RF modulator block, which is frequency-synthesizer based with an integrated VCO, generates the 5.8GHz band FM signal modulated with video signal and two modulated audio subcarriers at 6MHz and 6.5MHz respectively. Both Stereo and Mono application are available on the chip.

Transmission frequency can be set by internal register via SPI programming, or by selecting six dedicated pins. Two stages output power of +2dBm or +13dBm can be configured via pins 34 and 35. Both CE and FCC regulations are easy to pass by using RTC6705 with application circuit and single room shielding case.

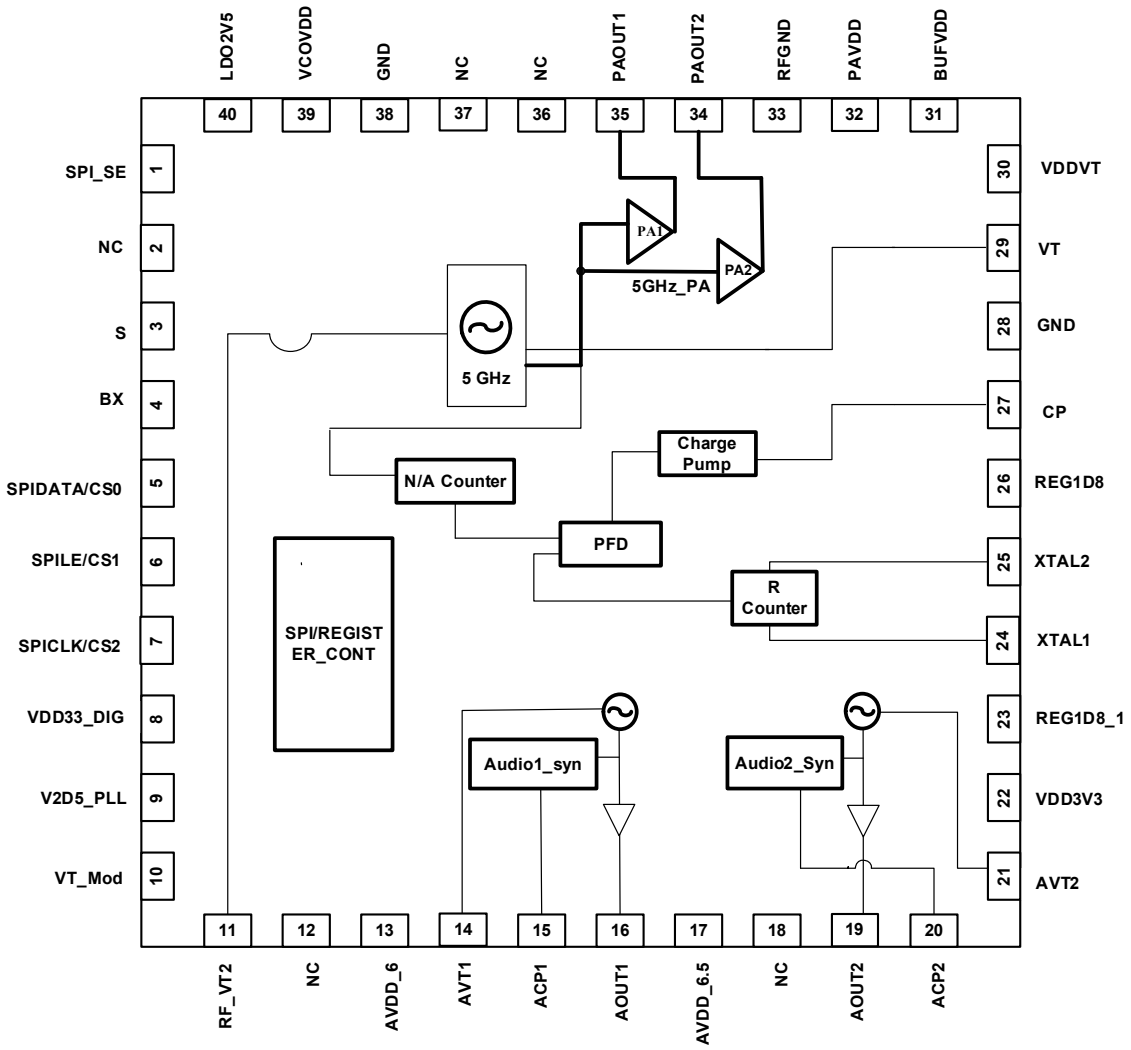
Features

- 3.3V power supply
- Built-in PA with +13dBm output power
- 5.8GHz band FM modulator and transmitter
- Simple digital pins setting 24 fixed channels to eliminate external micro-controller
- Two audio subcarrier modulators at 6MHz/6.5MHz
- Single chip CMOS technology with integrated VCO and PLL
- Transmitter frequency programmability by SPI
- 40-pin leadless QFN package pass RoHS

Application

- AV Sender
- Baby Monitor
- Wireless Camera
- Wireless Audio
- Wireless Earphone

Block Diagram



PIN	NAME	I/O	FUNCTION
1	SPI_SE	Digital IN	Switch mode or SPI selection[1]
2	NC		Not connected
3	S	Digital IN	A/B band selection[1] 0 for A band; 1 for B band
4	BX	Digital IN	Alternative band selection[1]
5	CS0	Digital IN	Easy Channel selection[1]
	SPIDATA	Digital IN	SPI digital control
6	CS1	Digital IN	Easy Channel selection[1]
	SPILE	Digital IN	SPI digital control
7	CS2	Digital IN	Easy channel selection[1]
	SPICLK	Digital IN	SPI digital control
8	VDD33_DIG	Supply IN	3.3V DC power supply
9	V2D5_PLL	Supply IN	3.3V DC power supply for audio modulator PLL
10	VT_Mod	Analog IN	Modulation input for Video
11	RF_VT2	Analog IN	Modulation input for audio subcarriers
12	NC		Not connected
13	AVDD_6	Supply IN	3.3V power supply for audio 6MHz VCO
14	AVT1	Analog IN	Vtune for audio 6MHz PLL
15	ACP1	Analog OUT	Charge pump for audio 6MHz
16	AOUT1	Analog OUT	FM modulated audio 6MHz output
17	AVDD_6.5	Supply IN	3.3V power supply for audio 6.5Mz VCO
18	NC		Not connected
19	AOUT2	Analog OUT	FM modulated audio 6.5MHz output
20	ACP2	Analog OUT	Charge pump for audio 6.5MHz
21	AVT2	Analog IN	Vtune for audio 6.5MHz PLL
22	VDD3V3	Supply IN	3.3V Analog power supply
23	REG1D8_1	Analog OUT	Regulator OUT 1.8V regulator output for audio
24	XTAL1	Analog I/O	Crystal connection
25	XTAL2	Analog I/O	Crystal connection
26	REG1D8	Analog OUT	Regulator OUT 1.8V regulator output for video
27	CP	Analog OUT	Synthesizer charge pump output
28	GND	Analog GND	Analog GND
29	VT	Analog IN	Vtune for VCO
30	VDDVT	Supply IN	3.3V Analog power supply
31	BUFVDD	Supply IN	3.3V Analog power supply for PA bias & buffer
32	PAVDD	Supply IN	3.3V VDD
33	RFGND	Analog GND	RF GND
34	PAOUT2	Analog OUT	PA output for 13dBm at 5.8GHz band
35	PAOUT1	Analog OUT	PA output for 2dBm at 5.8GHz band
36	NC		Not connected
37	NC		Not connected
38	GND	Analog GND	
39	VCOVDD	Supply IN	3.3V Analog power supply for VCO

40	LDD2V5	Supply IN	Analog power supply for VCO

Note 1. Internal pull-high circuit can be left floating for logical high.

ELECTRICAL SPECIFICATIONS

(1) Absolute Maximum Ratings

SYMBOL	PARAMETER	Ratings	UNIT
Tstr	Storage Temperature Range	-65 to +150	℃
Totr	Operating Temperature Range	-40 to +85	℃
Vdd	Supply Voltage	-0.5 to +5	V
Vlog	Logic control signal	-0.5 to +5	V
VRX	RX input	-2 to +2	V

The maximum rating must not be exceeded at any time. Do not operate the device under conditions outside the above

(2) DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Tj	Temperature Range	-	-40	25	85	℃
VDD	Supply Voltage		3.1	3.3	3.5	V
I_module high	Power consumption for reference design with 13dBm output power	TT 25C, 3.3V		100		mA
I_module low	Power consumption for reference design with 2dBm output power	TT 25C, 3.3V		TBD		mA
Icc	Power consumption for chip with 13dBm output power	TT 25C, 3.3V		95		mA
Fref	Oscillator operating frequency			8		MHz
V_IH	High Level Input Voltage for digital interface	V_IO=3V	0.7xV_IO		V_IO+0.3	V
V_IL	Low Level Input Voltage for digital interface		-0.3		0.3xV_IO	V

(3) 5GHz Band Transmitter Specifications (T 25℃, 3.3V)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Fc	Frequency Range	Temperature Range -40℃ to 85℃	5725		5865	MHz
Pout_H*	Maximum output power at high power mode with reference design	Connect PAOUT1 and PAOUT2		13		dBm
Pout_L*	Maximum output power at low power mode with reference design	Connect PAOUT1 only		2		dBm
PN	The phase noise at 5725GHz	100KHz offset 1MHz offset		-90 -115		dBc/Hz
2ndH_H*	The 2nd Harmonic referenced with the fundamental signal at high power mode	With reference filter design		-60		dBc

3rdH_H*	The 3rd Harmonic referenced with the fundamental signal at high power mode	With reference filter design		-60		dBc
2ndH_L*	The 2nd Harmonic referenced with the fundamental signal at low power mode	With reference filter design		-60		dBc
3rdH_L*	The 3rd Harmonic referenced with the fundamental signal at low power mode	With reference filter design		-60		dBc
* All with proper match at the PA output, before further ceramic filtering.						
Video						
Zin_video	Video input impedance			75		Ω
Vin_video	Video peak to peak input voltage (as reference design)			1		Vpp
Audio						
VTAA	Video carrier to audio carrier ratio (as reference design)	No video and audio signal in	-30	-25		dBc
fau	Audio carrier frequency	Left sound Right sound		6 6.5		MHz
THD	Total harmonic distortion	@1KHz tone input with ±25KHz frequency deviation		1		%
F_corner	3dB corner frequency of pre-emphasis (as reference design)			12		kHz
SNR_A	Audio SNR (as reference design,) With pre-emphasis/ de-emphasis,	@1KHz tone input with 2Vpp audio		56		dB

(4) SPI Digital Timing Diagram

In SPI Mode (**SPI_SE = 1**), the 3-wire SPI interface is used to configure the frequency as well as internal registers. Series data sequence of 3-wire SPI is shown in following Figure. This **25-bit** data stream consists of **4 address bits**, 1 read/write control bit and 20 data bits. Data transfer is LSB first.

During write cycle (R/W = 1), the chip will sample the **SPIDATA** on the rising edge of **SPICLK**. Sampled data will be temporally stored in internal shift register. One the rising edge of **SPILE**, data in shift register will be latched into specific register according to the address.

During read cycle (R/W = 0), address and read/write control bit are sampled at rising edge of **SPICLK**, but the data bits are sent at the falling edge of **SPICLK**.

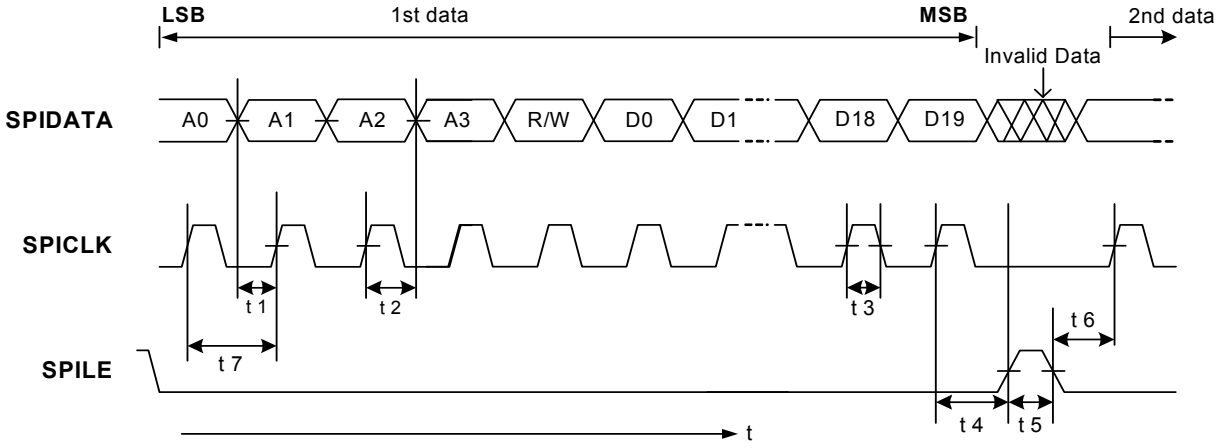


Figure 6.1 Series data sequence on SPI interface of RTC6716

Parameter	Min.	Typ.	Max.	Unit
t1	20	-	-	ns
t2	20	-	-	ns
t3	30	-	-	ns
t4	30	-	-	ns
t5	100	-	-	ns
t6	20	-	-	ns
t7	100	-	-	ns

Note:
1.) On the rising edge of the SPICLK, one bit of data is transferred into the shift register.
2.) SPILE should be “L” when the data is transferred into the shift register.

Channel Selection Table

When pin 1 (SPI_SE) is set at low voltage, the chip works as in the easy channel selection mode and the pins 5(SPIDATA/CS0), 6(SPILE/CS1), 7(SPICLK/CS2)，3(S) and 4(BX) are used for channel selection. Channel frequencies refer to below table.

	SPI_SE	Band	BX	S	CS[2:0]							
					000	001	010	011	100	101	110	111
5GHz Band	0	A	0	0	5865M	5845M	5825M	5805M	5785M	5765M	5745M	5725M
	0	B	0	1	5733M	5752M	5771M	5790M	5809M	5828M	5847M	5866M
	0	E	1	X	5705M	5685M	5665M	5645M	5885M	5905M	5925M	5945M
	1	SPI	X	X	three wire SPI control pins							

SPI mode

When pin 1 (SPI_SE) is set at high (3.3V), the chip works as in the SPI mode and the pins 5(SPIDATA/CS0), 6(SPILE/CS1) and 7(SPICLK/CS2) are used for 'SPI' inputs for 3-wire programming interface.

Register Definition

Address 0x00: Synthesizer Register A

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–					SYN_RF_R_REG [14:0]														
Default	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

SYN_RF_R_REG [14:0]:	R-counter divider ratio control for RF Synthesizer. Default: 400xD(= 00190xH) Crystal clock (F_{osc})=: 8MHz Reference clock=crystal clock/R-counter=8MHz/400=20KHz

Address 0x01: Synthesizer Register B

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYN_RF_N_REG [12:0]													SYN_RF_A_REG [6:0]						
5G Default	0	1	0	0	0	1	1	1	1	0	0	1	1	0	0	0	0	0	0	1

Synthesizer counter default setting(5.8Ghz band:5865MHz) For 5.8Ghz band, **F_{RF} = 2*(N*64+A)*(F_{osc}/R)** Example: default F_{RF}=5865MHz, F_{osc}=8MHz, R=400 5865=(2*N*64+A)*8Mhz/400=2*(N*64+A)*20KHz N=2291(=8F3xH), A=1(=01xH)	
SYN_RF_N_REG [12:0]:	N counter divider ratio control for RF Synthesizer
SYN_RF_A_REG [6:0]:	A counter divider ratio control for RF Synthesizer.

Address 0x02: Synthesizer Register C

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VREFADJ [2:0]			A1CT [7:0]								CP_FT [2:0]			SC_CTL	MOUT [1:0]		PRES_FT [2:0]		
Default	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1

VREFADJ [2:0]	Vref adjusting
A1CT [7:3:]	Audio modulator R counter value
A1CT [2:0]	Audio modulator charge pump current control
CP_FT [2:0]	Charge pump current control (from 50uA to 6mA, default=100uA) NOTE: DIG_CT shall set it to 111 for 6mA Icp.
SC_CTL:	CP current test control
MOUT [1:0]	Multi-function output select (RF R divider output, RF prescaler output, lock in detect)
PRES_FT [2:0]	Prescaler tail current control (20 ~ 140uA).

Address 0x03: RF VCO and DFC Control Register

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–			CAL_OK	R [9:0]										EX_CAP [5:0]					
5G Default	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1

CAL_OK:	VCO fine tune
R [9:0]:	VCO control
EX_CAP [5:0]:	VCO fine tune

Address 0x04: VCO Control Register

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BC_SEL [1:0]		MB5G [2:0]			VB_SEL5G [4:0]					VB4_KM5G [1:0]		VB3_KM5G [1:0]		VB2_KM5G [1:0]		VB1_KM5G [1:0]		VB0_KM5G [1:0]	
Default	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BC_SEL [1:0]:	Bias Center Control
MB5G [2:0]:	5G VCO control
VB_SEL5G [4:0]:	5G VCO adjustment
VB4_KM5G [1:0]:	5G VCO adjustment
VB3_KM5G [1:0]:	5G VCO adjustment
VB2_KM5G [1:0]:	5G VCO adjustment
VB1_KM5G [1:0]:	5G VCO adjustment
VB0_KM5G [1:0]:	5G VCO adjustment

Address 0x05: VCO Control Register

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TC_BUF2G [1:0]		MB2G [2:0]			VB_SEL2G [4:0]					VB4_KM2G [1:0]		VB3_KM2G [1:0]		VB2_KM2G [1:0]		VB1_KM2G [1:0]		VB0_KM2G [1:0]	
Default	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TC_BUF2G [1:0]:	VCOBUF current control
MB2G [2:0]:	VCO current control
VB_SEL2G [4:0]:	VCO adjustment
VB4_KM2G [1:0]:	VCO adjustment
VB3_KM2G [1:0]:	VCO adjustment
VB2_KM2G [1:0]:	VCO adjustment
VB1_KM2G [1:0]:	VCO adjustment
VB0_KM2G [1:0]:	VCO adjustment

Address 0x06: Audio Modulator Control Register

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–		MB_6M [3:0]				VCO6M_D [4:0]					MB_6M5 [3:0]				VCO6M5_D [4:0]				
Default	0	0	0	1	1	1	0	1	1	1	1	0	1	1	1	0	1	1	1	1

MB_6M [2:0]:	6M VCO control
VCO6M_D [4:0]:	6M VCO control code
MB_6M5 [2:0]:	6M5 VCO control
VCO6M5_D [4:0]:	6M5 VCO control code

Address 0x07: Pre-driver and PA Control Register

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAI_5G [4:0]					DP_5G [2:0]			PA5G_BS [2:0]			PA5G_PW [1:0]		PD_Q5G	QI_5G [2:0]			PA_BS [2:0]		
Default	0	0	0	0	0	1	0	0	1	1	1	1	1	0	1	1	1	1	0	1

MAI_5G [4:0]:	5G Pre-driver output control;
DP_5G [2:0]:	5G Pre-driver gain/linearity control
PA5G_BS [2:0]:	5G PA gain control
PA5G_PW [1:0]:	5G PA output power control
PD_Q5G:	Power down 5G pre-driver control
QI_5G [2:0]:	5GHz pre-driver control
PA_BS [2:0]:	PA gain control

Address 0x08 ~ 0x0E: Reserved

Address 0x0F: State Register

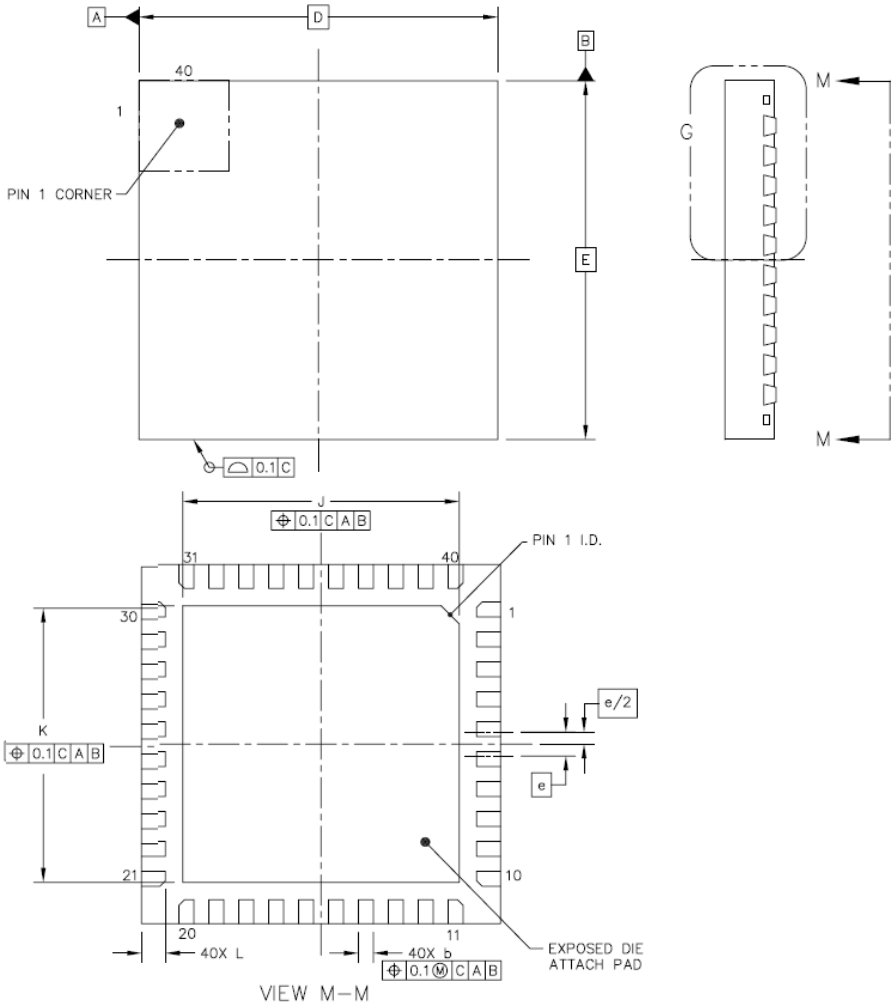
Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–																	STATE [2:0]		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

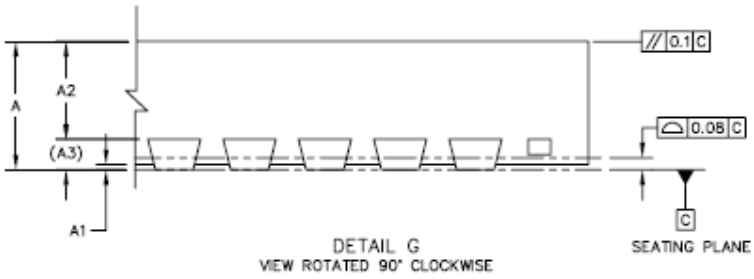
STATE [2:0]: Current State of the chip.

STATE [2:0]	State Name	Description
000	RESET	Reset state.
001	PWRON_CAL	Power on state.
010	STBY	Standby state.
011	VCO_CAL	VCO state.
100~111	Reserved	

PACKAGE

QFN 6X6 40 pins





DIM	MIN	NOM	MAX
A	0.8	0.85	0.9
A1	0	0.035	0.05
A2	---	0.65	0.67
A3		0.203 REF.	
b	0.2	0.25	0.3
D		6 BSC	
E		6 BSC	
e		0.5 BSC	
J	4.52	4.62	4.72
K	4.52	4.62	4.72
L	0.35	0.4	0.45

NOTES

1.0 COPLANRITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
MM	ASME Y14.5M	---